1024 BIT DYNAMIC SHIFT REGISTER

- **Guaranteed 5 MHz Operation over Temperature Range**
- **Low Power Dissipation --.1 mW/bit at 1 MHz**
- **DTL, TTL Compatible**
- **Low Clock Capacitance -- 140 pF**
- **Low Clock Leakage -- ≤ 1 μA**
- **Inputs Protected Against Static Charge**
- **Standard Packaging -- 8 Lead Metal Can, 16 Pin Ceramic Dual In-Line**
- **Three Standard Configurations -- Quad 256 Bit -- 1402A, Dual 512 Bit -- 1403A, Single 1024 Bit -- 1404A**

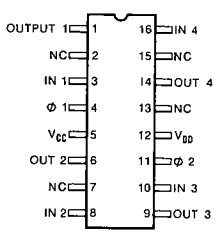
The 1402A/1403A/1404A are direct pin for pin replacements for the 1402/1403/1404. Due to "on chip" multiplexing the data rate is twice the clock rate. Data is shifted one bit on each clock pulse (both ϕ_1 and ϕ_2).

The 1402A/1403A/1404A family is ideally suited for usage in low cost serial memories or delay line applications. A high speed data rate of 5 MHz is easily obtained at the power supplies of +5V and −5V. The 1402A/3A/4A are capable of operating at the power supply voltages of +5V, −9V as well as +5V, −5V.

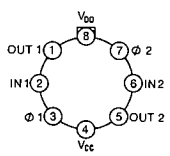
The input to the shift register can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The design of the output stage provides driving capability for both MOS and bipolar IC's.

Use of low threshold **silicon gate technology** allows high speed (5 MHz guaranteed) while reducing power dissipation by a factor of **two** and clock input capacitance by a factor of **three** compared to equivalent products manufactured by conventional technologies.

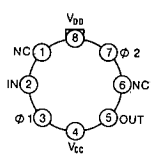
PIN CONFIGURATION



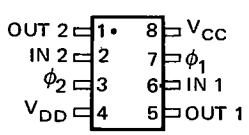
C1402A/P1402A



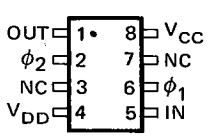
M1403A



M1404A



P1403A



P1404A

Absolute Maximum Ratings[1]

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
Power Dissipation[2]	1 Watt
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V

D.C. Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ±5% or −9V ±5%

SYMBOL	TEST	MIN.	TYP[3]	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current		<10	500	nA	T_A =25°C
I_{LO}	Output Leakage Current		<10	1000	nA	V_{OUT}=0.0V, T_A=25°C
I_{LC}	Clock Leakage Current		10	1000	nA	Max. V_{ILC}, T_A=25°C
V_{IL}	Input "Low" Voltage	V_{CC}−10		V_{CC}−4.2	V	
V_{IH}	Input "High" Voltage	V_{CC}−2		V_{CC}+.3	V	

V_{DD} = −5V ±5%

I_{DD1}	Power Supply Current		40	50	mA	T_A=25°C; Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −17V
I_{DD2}	Power Supply Current			56	mA	T_C=0°C; Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −17V
V_{ILC}	Clock Input Low Voltage	V_{CC}−17		V_{CC}−15	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1}=3K to V_{DD}, I_{OL}= 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1}=3K to V_{DD}, I_{OH}=−100 µA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.6	V_{CC}−1		V	R_{L2}=4.7K to V_{DD} (See p. 6 for connection)

V_{DD} = −9V ±5%

I_{DD3}	Power Supply Current		30	40	mA	T_A=25°C; Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −14.7V
I_{DD4}	Power Supply Current			45	mA	T_C=0°C; Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −14.7V
V_{ILC}	Clock Input Low Voltage	V_{CC}−14.7		V_{CC}−12.6	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1}=4.7K to V_{DD}, I_{OL}= 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1}=4.7K to V_{DD}, I_{OH}=−100µA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.9	V_{CC}−1		V	R_{L2}=6.2K to V_{DD}, R_{L3}=3.9K to V_{CC} (See p. 6 for connection)

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 3. When operating at V_{DD} = −5V±5% the maximum duty cycle is 33% and at V_{DD}=−9V+5% the maximum duty cycle is 26%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$x clock rate.

Note 3: Typical values are at T_A = 25°C and at nominal voltages.

A.C. Characteristics T_A = 0°C to 70°C; V_{CC} = +5V ±5%

SYMBOL	TEST	V_{DD} = −5V ±5% (Test Load 1)		V_{DD} = −9V ±5% (Test Load 2)		UNIT
		MIN.	MAX.	MIN.	MAX.	
Frequency	Clock Rep Rate		2.5		1.5	MHz
Frequency	Data Rep Rate	Note 1	5.0	Note 1	3.0	MHz
$t_{\phi PW}$	Clock Pulse Width	.130	10	.170	10	μsec
$t_{\phi D}$	Clock Pulse Delay	10	Note 1	10	Note 1	nsec
t_R, t_F	Clock Pulse Transition		1000		1000	nsec
t_{DW}	Data Write Time (Set Up)	30		60		nsec
t_{DH}	Data To Clock Hold Time	20		20		nsec
t_{A+}, t_{A-}	Clock To Data Out Delay		90		110	nsec

CAPACITANCE[2] V_{CC} = +5V ±5%, V_{DD} = −5V ±5% or −9V ±5%, T_A = 25°C

SYMBOL	TEST	TYP.	MAX.	CONDITIONS	
C_{IN}	Input Capacitance	5 pF	10 pF	$V_{IN} = V_{CC}$	f = 1 MHz
C_{OUT}	Output Capacitance	5 pF	10 pF	$V_{OUT} = V_{CC}$	
C_ϕ	Clock Capacitance	110 pF	140 pF	$V_\phi = V_{CC}$	
$C_{\phi 1\,\phi 2}$	Clock to Clock Capacitance	11 pF	16 pF	$V_\phi = V_{CC}$	

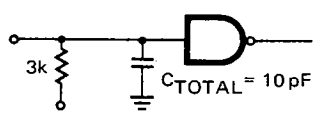
Note 1: See page 5 for guaranteed curve. Note 2: This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test

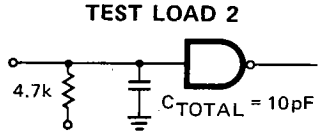
Input rise and fall times: 10 nsec
Output load is 1 TTL gate

TEST LOAD 1



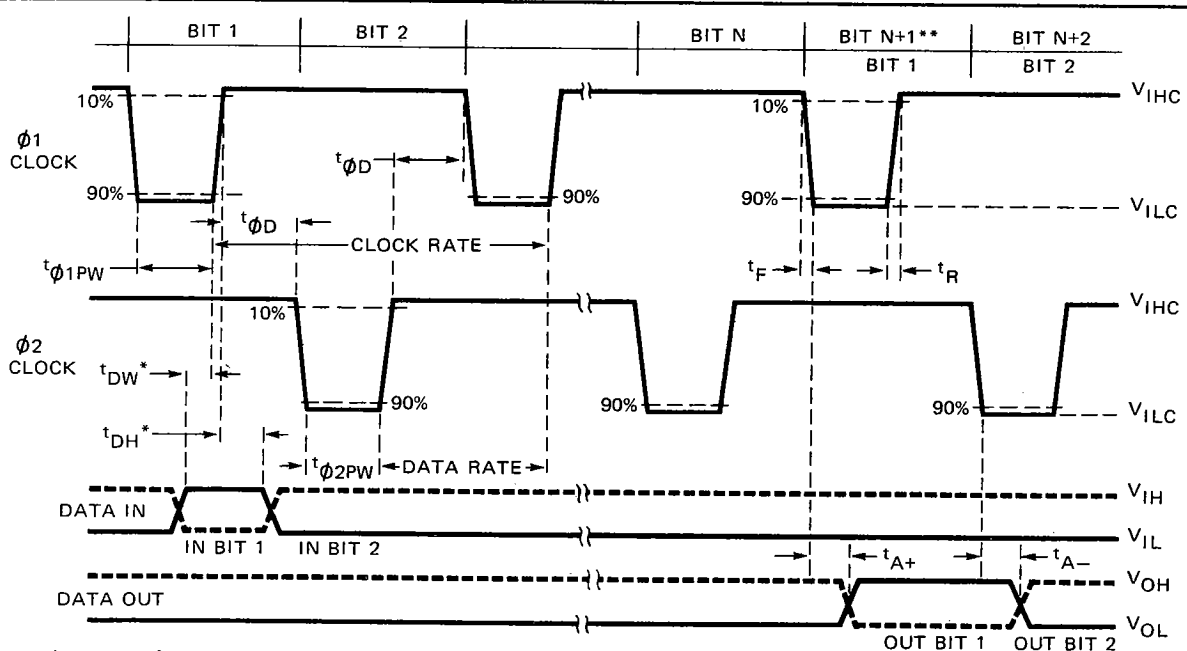
V_{DD} = −5V ±5%

TEST LOAD 2



V_{DD} = −9V ±5%

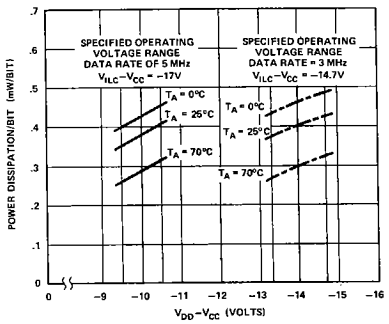
Timing Diagram



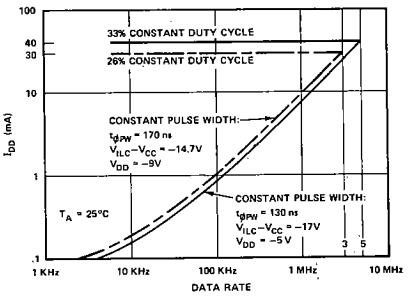
*t_{DW} and t_{DH} same for $t_{\phi 2}$ **N = 256 for 1402A, N = 512 for 1403A, N = 1024 for 1404A

Typical Characteristics

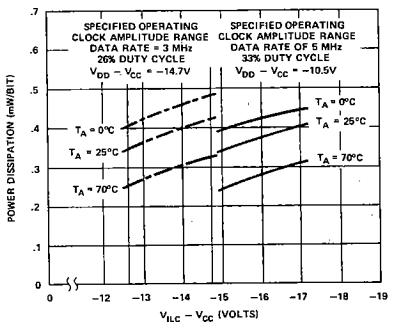
POWER DISSIPATION / BIT VS SUPPLY VOLTAGE



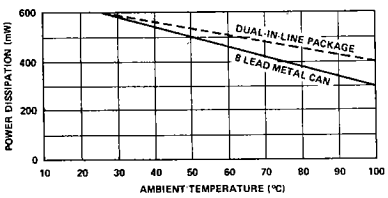
I_{DD} CURRENT VS DATA RATE



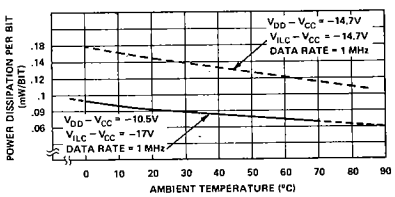
POWER DISSIPATION / BIT VS CLOCK AMPLITUDE



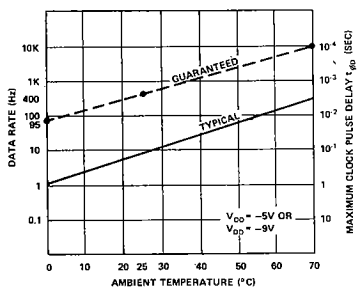
MAXIMUM ALLOWABLE POWER DISSIPATION



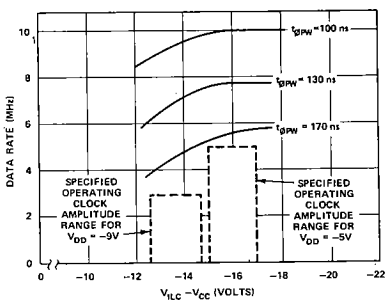
POWER DISSIPATION / BIT VS TEMPERATURE



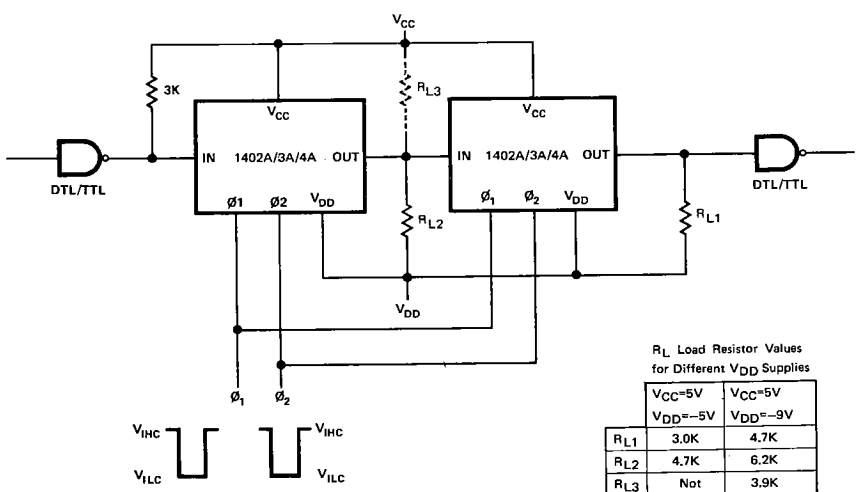
MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS TEMPERATURE



MAXIMUM DATA RATE VS CLOCK AMPLITUDE



DTL/TTL MOS Interfaces



R_L Load Resistor Values for Different V_{DD} Supplies

	V_{CC}=5V V_{DD}=−5V	V_{CC}=5V V_{DD}=−9V
R_{L1}	3.0K	4.7K
R_{L2}	4.7K	6.2K
R_{L3}	Not required	3.9K