TYPES SN74S428(TIM8228), SN74S438(TIM8238)
CONTROLLER AND BUS DRIVER FOR 8080A SYSTEMS

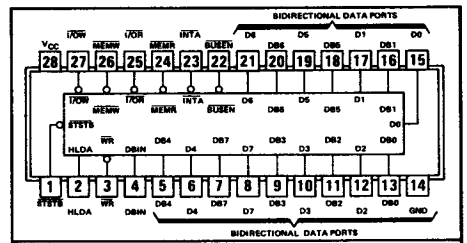
BULLETIN NO. DL-S 12468, OCTOBER 1976

- **Designed to Be Interchangeable with Intel 8228 and 8238**

PIN DESIGNATIONS

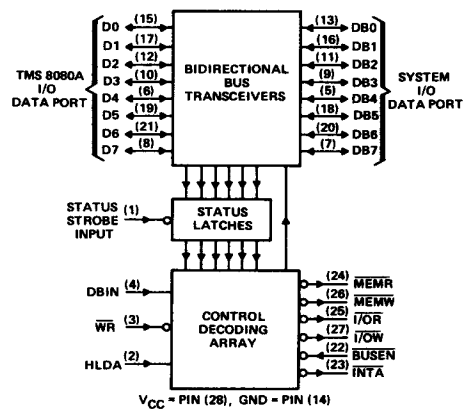
DESIGNATION	PIN NOS.	FUNCTION
D0 thru D7	15, 17, 12, 10, 6, 19, 21, 8	BIDIRECTIONAL DATA PORT (TO TMS 8080A)
DB0 thru DB7	13, 16, 11, 9, 5, 18, 20, 7	BIDIRECTIONAL DATA PORT (TO SYSTEM BUS)
$\overline{I/OR}$	25	READ OUTPUT TO I/O (ACTIVE LOW)
$\overline{IO/W}$	27	WRITE OUTPUT TO I/O (ACTIVE LOW)
$\overline{MEMR}$	24	READ OUTPUT TO MEMORY (ACTIVE LOW)
$\overline{MEMW}$	26	WRITE OUTPUT TO MEMORY (ACTIVE LOW)
DBIN	4	INPUT TO INDICATE TMS 8080A IS IN INPUT MODE (ACTIVE HIGH)
$\overline{INTA}$	23	INTERRUPT ACKNOWLEDGE OUTPUT (ACTIVE LOW)
HLDA	2	HOLD ACKNOWLEDGE INPUT (ACTIVE HIGH) FROM TMS 8080A
$\overline{WR}$	3	INPUT TO INDICATE TMS 8080A IS IN WRITE MODE (ACTIVE LOW)
$\overline{BUSEN}$	22	SYSTEM DATA PORT ENABLE INPUT (ACTIVE LOW)
$\overline{STSTB}$	1	SYNCHRONIZING STATUS STROBE INPUT FROM SN74LS424 (TIM8224)
V_{CC}	28	SUPPLY VOLTAGE (5 V)
GND	14	GROUND

N PACKAGE
(TOP VIEW)



logic: see description

functional block diagram



description

These monolithic Schottky-clamped †TTL system controllers are designed specifically to provide bus-driving and peripheral-control capabilities for interfacing memory and I/O devices with the 8080A in small to medium-large microcomputer systems.

A bidirectional eight-bit parallel bus driver is provided that isolates the 8080A bus from the memory and I/O data bus allowing the system designed to utilize cost-effective memory and peripheral devices while obtaining the maximum efficiency from the microprocessor. The TTL system drivers also provide increased fan-out with a lower impedance that enhances noise margins on the system bus.

Implementation of the status latches and control decoding array of the SN74S428/SN74S438 provides for using either a single-level interrupt vector RST7 for small systems, or multiple-byte call instructions for systems needing unlimited interrupt levels.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

description (continued)

With respect to the system clocks, the SN74S438 is configured to generate an advanced response for I/O or memory write output signals to further simplify peripheral control implementation of complex systems. See Figure 3.

8-bit parrallel bus transceiver

The 8-bit parallel bus transceiver buffers the 8080A data bus from the memory and I/O system bus by providing one port (DO through D7) to interface with the 8080A and another port (DBO through DB7) to interface with the system devices. The 8080A side of the transceiver is designed specifically to interface with the microprocessor data bus ensuring not only that the processor output drive capabilities are adequate, but also that the inputs are driven with enhanced noise margins. The system bus side features high fan-out buffers designed to drive a number of system devices simultaneously and directly. The system port is rated to sink ten milliamperes of current and to source one milliampere of current at standard low-threshold voltage levels.

Status lines from the 8080A instruction-status decoder and the system bus enable input (BUSEN) provide complete transceiver directional and enable control to ensure integrity of both the processor data and the system bus data.

status latches

During the beginning of each machine cycle, the six status latches receive status information from the 8080A data bus indicating the type of operation that will be performed. When the $\overline{\text{STSTB}}$ input goes low, the latches store the status data and generate the signals needed to enable and sequence the memory and I/O control outputs. The status words and types of machine cycles are enumerated in Table A.

TABLE A – STATUS WORDS

STATUS WORD	8080A STATUS OUTPUT								TYPE OF MACHINE CYCLE	'S428/'S438 COMMAND GENERATED
	D0	D1	D2	D3	D4	D5	D6	D7		
1	L	H	L	L	L	H	L	H	Instruction fetch	$\overline{\text{MEMR}}$
2	L	H	L	L	L	L	L	H	Memory read	$\overline{\text{MEMR}}$
3	L	L	L	L	L	L	L	L	Memory write	$\overline{\text{MEMW}}$
4	L	H	H	L	L	L	L	H	Stack read	$\overline{\text{MEMR}}$
5	L	L	H	L	L	L	L	L	Stack write	$\overline{\text{MEMW}}$
6	L	H	L	L	L	L	H	L	Input read	$\overline{\text{I/OR}}$
7	L	L	L	L	H	L	L	L	Output write	$\overline{\text{I/OW}}$
8	H	H	L	L	L	H	L	L	Interrupt acknowledge	$\overline{\text{INTA}}$
9	L	H	L	H	L	L	L	H	Halt acknowledge	NONE
10	H	H	L	H	L	H	L	L	Interrupt acknowledge at halt	$\overline{\text{INTA}}$
	INTA	$\overline{\text{WO}}$	STACK	HLTA	OUT	M1	INP	MEMR		
	STATUS INFORMATION									

decoding array

The decoding array receives enabling commands from the status latches and sequencing commands from the 8080A and generates memory and I/O read/write commands and an interrupt acknowledgement.

description (continued)

The read commands ($\overline{\text{MEMR}}$, $\overline{\text{I/OR}}$) and the interrupt acknowledgement ($\overline{\text{INTA}}$) are derived from the status bit(s) and the data bus input mode (DBIN) signal. The write commands ($\overline{\text{MEMW}}$, $\overline{\text{I/OW}}$) are derived from the status bit(s) and the write mode ($\overline{\text{WR}}$) signal. (See Table A.) All control commands are active low to simplify interfacing with memory and I/O controllers.

The interrupt acknowledgement ($\overline{\text{INTA}}$) command output is actually a dual function pin. As an output, its function is to provide the $\overline{\text{INTA}}$ command to the memory and I/O peripherals as decoded from the status inputs and latches. When CALL is used as an interrupt instruction, the SN74S428/SN74S428 generates the proper sequence of control signals. Additionally, the terminal includes high-threshold decoding logic that permits it to be biased through a one-kilohm series resistor to the 12-volt supply to implement an interrupt structure that automatically inserts an RST7 instruction on the bus when the DBIN input is active and an interrupt is acknowledged. This capability provides a single-level interrupt vector with minimal hardware.

The asynchronous bus enable ($\overline{\text{BUSEN}}$) input to the decoding array is a control signal that protects the system bus. The system bus can be accessed and driven from the SN74S428/SN74S428 controller only when the $\overline{\text{BUSEN}}$ input is at a low voltage level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	D0 thru D7			−10	μA
	All others			−1	mA
Low-level output current, I_{OL}	D0 thru D7			2	mA
	All others			10	
Status strobe pulse width, $t_{w(STSTB)}$ (see Figure 3)		22			ns
Setup time, t_{su} (see Figure 3)	Status inputs D0 thru D7	8			ns
	System bus inputs to HLDA	10			
Hold time, t_h (see Figure 3)	Status inputs D0 thru D7	5			ns
	System bus inputs to HLDA	20			
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −5 mA			−1	V
V_{OH}	High-level output voltage	D0 thru D7	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	3.6	4		V
		All other outputs			2.4			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.45	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_O = 5.25 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_O = 0.45 V			−100	μA
I_{IH}	High-level input current	$\overline{INTA}$	V_{CC} = MIN,	See Figure 1			5	mA
		D0 thru D7	V_{CC} = MAX,	V_I = 5.25 V			20	μA
		All other inputs					100	
I_{IL}	Low-level input current	D2 or D6	V_{CC} = MAX,	V_I = 0.45 V			−750	μA
		$\overline{STSTB}$					−500	
		All other inputs					−250	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−15		−90	mA
I_{CC}	Supply current		V_{CC} = MAX			140	190	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see figure 3

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	D0 thru D7	DB0 thru DB7	C_L = 100 pF,	See Figure 2	5		40	ns
t_{PD}	DB0 thru DB7	D0 thru D7	C_L = 25 pF,	See Figure 2			30	ns
t_{PHL}	$\overline{STSTB}$	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$, $\overline{I/OW}$, $\overline{MEMW}$	C_L = 100 pF,	See Figure 2	20		60	ns
t_{PD}	$\overline{WR}$	$\overline{I/OW}$, $\overline{MEMW}$			5		45	ns
t_{PLH}	DBIN	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$					30	ns
t_{PLH}	HLDA	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$					25	ns
t_{PZX}	DBIN	D0 thru D7	C_L = 25 pF,	See Figure 2			45	ns
t_{PXZ}	DBIN	D0 thru D7					45	ns
t_{PZX}	$\overline{STSTB}$, $\overline{BUSEN}$	DB0 thru DB7	C_L = 100 pF,	See Figure 2			30	ns
t_{PXZ}	$\overline{BUSEN}$	DB0 thru DB7					30	ns

¶t_{PD} ≡ propagation delay time
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PZX} ≡ output enable time from high-impedance state
t_{PXZ} ≡ output disable time to high-impedance state

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PARAMETER MEASUREMENT INFORMATION

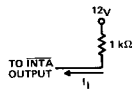


FIGURE 1—$\overline{\text{INTA}}$ INPUT CURRENT TEST CIRCUIT

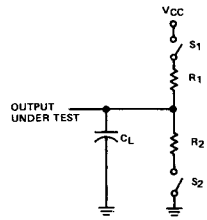
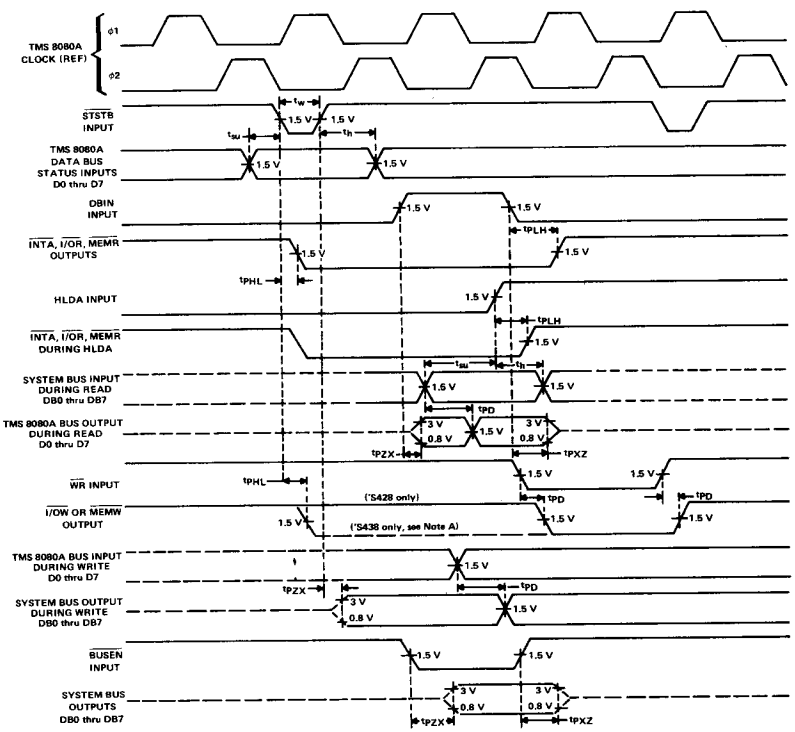


FIGURE 2—SWITCHING CHARACTERISTICS LOAD CIRCUIT



NOTE A: Advanced response of $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ for the SN74S438 is indicated by the dashed line.

FIGURE 3—VOLTAGE WAVEFORMS

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TYPICAL APPLICATION DATA

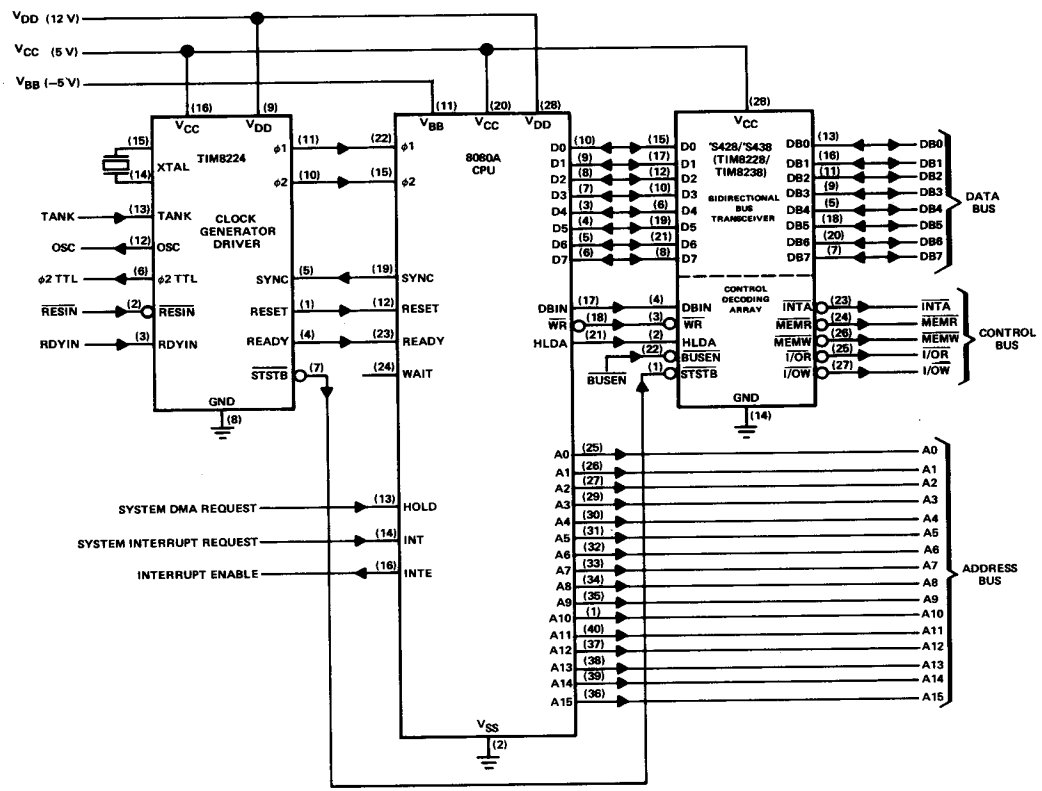

FIGURE 4—SYSTEM INTERFACING WITH CENTRAL PROCESSING UNIT