

PASIC FPGA FAMILIES

HIGH-SPEED, LOW POWER, INSTANT-ON, HIGH SECURITY FPGAs



PASIC FAMILY HIGHLIGHTS

- High performance (over 400 MHz)
- 100% routability and pin stability
- Instant-On capability
- High security and reliability
- Low power
- Available in commercial, industrial and military temperature grades
- Supports 5.0V, 3.3V and mixed-voltage systems

QuickLogic's three families of FPGAs — pASIC® 1, 2 and 3 — deliver high performance, low power and low cost, while maintaining the flexibility of customer-programmable parts. Built on the company's patented ViaLink® metal-to-metal interconnect technology, pASIC devices operate at speeds as high as 400MHz and have logic capacities up to 75,000 system gates.

The devices are architected to provide 100% routability with fixed pin-outs, as well as the highest level of system security and reliability. pASIC FPGAs are available in commercial, industrial and military temperature grades. All three pASIC families are supported by a variety of QuickLogic and third-party design tools.

Devices	System Gates	Logic Cells	Max. I/Os	Packages	Supply Voltage
pASIC 3					
QL3004	5,188	96	82	68-PLCC, 84-PLCC 100-TQFP	3.3V
QL3012	15,740	320	118	84-PLCC, 100-TQFP, 144-TQFP	3.3V
QL3025	32,616	672	204	144-TQFP, 208-PQFP, 256-PBGA	3.3V
QL3040	48,384	1,008	252	208-PQFP, 456-PBGA	3.3V
QL3060	75,232	1,584	316	208-PQFP, 456-PBGA	3.3V
pASIC 2					
QL2003	9,916	192	118	84-PLCC, 100-TQFP, 144-TQFP	5.0/3.3V
QL2005	16,120	320	156	84-PLCC, 144-TQFP, 208-PQFP	5.0/3.3V
QL2007	23,580	480	174	84-PLCC, 144-TQFP, 208-PQFP	5.0/3.3V
QL2009	32,826	672	225	144-TQFP, 208-PQFP, 256-PBGA	5.0/3.3V
pASIC 1					
QL8x12B	3,344	96	64	44-PLCC, 68-PLCC, 100-TQFP	5.0V
QL12x16B	6,608	192	88	68-PLCC, 84-PLCC, 100-TQFP	5.0V
QL16x24B	13,108	384	122	84-PLCC, 100-TQFP, 144-TQFP	5.0V
QL24x32B	26,088	768	180	144-TQFP, 208-PQFP	5.0V

HIGH PERFORMANCE — OVER 400 MHZ

QuickLogic created the revolutionary ViaLink metal-to-metal interconnect technology to deliver some of the world's fastest and easiest-to-use FPGAs. ViaLink elements establish high-speed logical and routing paths inside the devices by lowering resistance from over 1 gigaohm to less than 50 ohms when programmed. Unprogrammed connections feature extremely small capacitances, creating low RC signal delays and very high design performance.

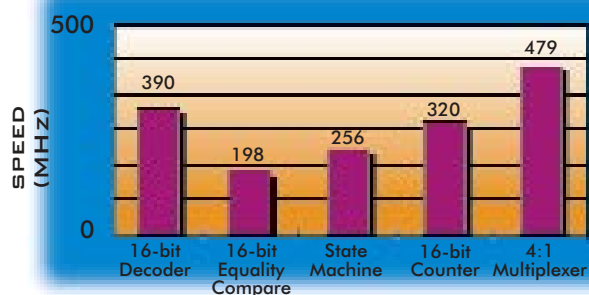
100% ROUTABILITY AND PIN STABILITY

The ViaLink interconnect is physically very small - resulting in fully populated routing intersections with small die sizes. The fully populated interconnect scheme used in pASIC devices is combined with abundant routing tracks to enable 100% routability for the user and the ability to define and maintain the same pin assignments during the entire development cycle. These benefits enable 100% gate utilization, minimal timing changes and short design cycles.

HIGH SECURITY AND RELIABILITY

Due to the non-volatility of QuickLogic's ViaLink technology, FPGA configuration information is completely self-contained, secure and reliable. There is no need for an external "boot PROM", saving valuable board real-estate and preventing your intellectual property from being copied or stolen. QuickLogic FPGAs also provide the highest system reliability, since they are live at power-up and eliminate the risk of losing data.

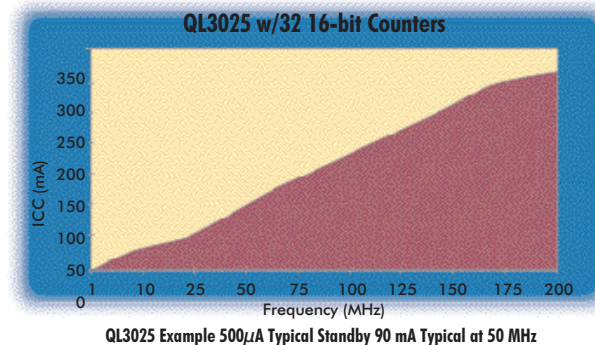
DEVICE PERFORMANCE



The unique combination of QuickLogic's technology and architecture results in the highest system-level performance.

LOW POWER

Because the ViaLink interconnect's impedance is so low, pASIC devices consume less power than most FPGAs, and much less than equivalent-density CPLDs. Typical standby power consumption for the pASIC 3 family is as low as 500 μ A, with QL3025 designs commonly drawing less than 100mA at 50MHz.



ViaLink interconnect requires very low power, even at high operating frequencies.

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