

FEATURES

- Extended Operating Temperature Range
($-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$)
- Address Activated™ Interface combines benefits of Edge Activated™ and full static
- High performance
- TTL compatible I/O
Fanout: 2 - Standard
2 - Standard TTL
2 - Schottky TTL
12 - Low power Schottky TTL
- Low Power - 400mW Active
- 24-pin ROM/PROM compatible pin configuration
- $\overline{\text{CS}}$, $\overline{\text{OE}}$, and $\overline{\text{LATCH}}$ functions for flexible system operation
- Read-Modify-Write Capability
- Single +5 volt power supply
- Ruggedized for use in severe military environment

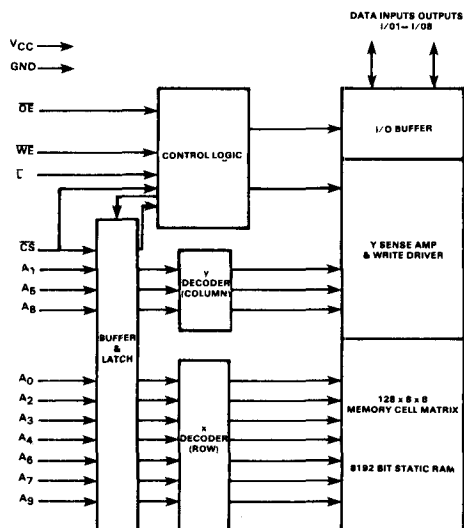
PART NUMBER	ACCESS TIME	CYCLE TIME
MKB4118-82	150 nsec	150 nsec
MKB4118-83	200 nsec	200 nsec

DESCRIPTION

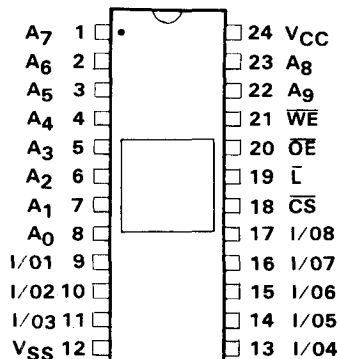
The MKB4118 uses Mostek's Poly R N-Channel Silicon Gate process and advanced circuit design techniques to package 8192 bits of static RAM on a single chip. Mostek's Address Activated™ circuit design technique

is utilized to achieve higher performance, low power, and easy user implementation. The device has a $V_{IH} = 2.2$, $V_{IL} = 0.8\text{V}$, $V_{OH} = 0.4\text{V}$ making it totally compatible with all TTL family devices.

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A0 - A9	Address Inputs	WE	Write Enable
CS	Chip Select	OE	Output Enable
VSS	Ground	LATCH	Latch
VCC	Power (+5V)	I/O1 I/O8	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature (Ambient)(Ceramic)	–65°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS³

(–55°C ≤ T_C ≤ +125°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3		.8	V	1

DC ELECTRICAL CHARACTERISTICS^{1,3}

(–55°C ≤ T_C ≤ +125°C) (V_{CC} = 5.0 Volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current (Active)		100	mA	
I_{CC2}	Average V_{CC} Power Supply Current (Standby)		80	mA	5
I_{IL}	Input Leakage Current (Any Input)	–10	10	μA	2
I_{OL}	Output Leakage Current	–10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = –1mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS^{1,3}

(–55°C ≤ T_C ≤ +125°C) (V_{CC} = +5.0 Volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins except I/O	4pF		4
$C_{I/O}$	Capacitance on I/O pins	10pF		4

NOTES:

1. All voltages referenced to V_{SS} .
2. Measured with $0 \leq V_I \leq 5V$ and outputs deselected (V_{CC} = 5V)
3. A minimum of 2ms time delay is required after application of V_{CC} (+5V) before proper device operation can be achieved.
4. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} nominal
5. Standby mode is defined as condition with addresses, latch and WE remain unchanged.
6. AC timing measurements made with 2 TTL loads plus 100pF.

ELECTRICAL CHARACTERISTICS^a

(-55°C ≤ T_C ≤ 125°C and V_{CC} = 5.0 Volts ± 5%)

SYM	PARAMETER	MKB4118-82		MKB4118-83		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t _{RC}	Read Cycle Time	150		200		ns	
t _{AA}	Address Access Time		150		200	ns	
t _{CSA}	Chip Select Access Time		75		100	ns	
t _{CSZ}	Chip Select Data Off Time	0	75	0	100	ns	
t _{OEA}	Output Enable Access Time		75		100	ns	
t _{OEZ}	Output Enable Data Off Time	0	75	0	100	ns	
t _{AZ}	Address Data Off Time	10		10		ns	
t _{ASL}	Address to Latch Setup Time	10		10		ns	
t _{AHL}	Address From Latch Hold Time	50		65		ns	
t _{CSL}	CS To Latch Setup Time	0		0		ns	
t _{CHL}	CS From Latch Hold Time	50		65		ns	
t _{LA}	Latch Off Access Time		200		260	ns	
t _{WC}	Write Cycle Time	150		200		ns	
t _{ASW}	Address To Write Setup Time	0		0		ns	
t _{AHW}	Address From Write Hold Time	50		65		ns	
t _{CSW}	CS to Write Setup Time	0		0		ns	
t _{CHW}	CS From Write Hold Time	50		65		ns	
t _{DSW}	Data to Write Setup Time	30		40		ns	
t _{DHW}	Data From Write Hold Time	30		40		ns	
t _{WD}	Write Pulse Duration	50		60		ns	
t _{LDH}	Latch Duration, High	50	DC	60	DC	ns	
t _{LDL}	Latch Duration, Low		DC		DC	ns	
t _{WEZ}	Write Enable Data Off Time	0	75	0	100	ns	
t _{LZ}	Latch Data Off Time	10		10		ns	
t _{WPL}	Write Pulse Lead Time	90		130		ns	

**SUPPLEMENTAL DATA SHEET TO BE USED IN
CONJUNCTION WITH MOSTEK MK4118(P/N) SERIES DATA SHEET**

The MKB4118 is designed for all wide word memory applications. The MKB4118 provides the user with a high-density, cost-effective 1K x 8 bit Random Access Memory. Fast Output Enable ($\overline{OE}$) and Chip Select ($\overline{CS}$) controls are provided for easy interface in micro-processor or other bus-oriented systems. The MKB4118 features a flexible Latch ($\overline{L}$) function to permit latching of

the address and $\overline{CS}$ status at the user's option. Common data address bus operation may be performed at the system level by utilizing the L and $\overline{OE}$ functions for the MKB4118. The latch function may be bypassed by merely tying the latch pin to V_{CC} , providing fast ripple-through operation.